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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/434,654	11/05/1999	KEVIN J RYAN	303.306US4	4209

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EXAMINER	
PEIKARI, BEHZAD	

ART UNIT	PAPER NUMBER
2186	

DATE MAILED: 08/05/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/434,654	RYAN, KEVIN J	
	Examiner	Art Unit	
	B. James Peikari	2186	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01 July 2003* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *13-16 and 32-60* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *13-16 and 32-60* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *20* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Drawings

1. The application includes informal drawing Figures that are suitable for examination purposes, i.e., the proposed Figure 6 submitted with the amendment of October 15, 2002. Formal drawings will be required until the application is allowed.

Claim Rejections - 35 USC § 103

- In the amendment filed on July 22, 2002, applicant admitted on page 1 that the contents of Figure 6 (namely a DRAM containing its own row decoder, column decoder, data in buffer and data out buffer) are believed to contain no new matter. However, since the disclosure never supported this feature prior to the proposed Figure 6, stating that this feature is not new matter is equivalent to an admission that a DRAM containing its own row decoder, column decoder, data in buffer and data out buffer was prior art.

Furthermore, applicant's submission, in a copending application, of pages 2 and 9 of *DRAM Circuit Design* (showing a DRAM containing its own row decoder, column decoder, data in buffer and data out buffer) as evidence of what is well known serves as further evidence that this feature was prior art.

Consequently, In the Office action mailed December 26, 2002, a new rejection was made that treated this feature as well known prior art. These same grounds of rejection is hereby maintained and repeated below, with further explanation of the features noted by applicant in the response filed on July 1, 2003.

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 13-16 and 32-60 are rejected under 35 U.S.C. 103(a) as being unpatentable over Katayama et al., U.S. 5,875,452, in view of Rosich et al., U.S. 5,587,964.

Katayama et al. teach the claimed invention in a memory system (*note especially Figure 9*) comprising:

a memory controller (*note memory controller 17, via controller 70*) with a unidirectional command and address bus (*note that the address and control lines from controller 70 to the decoders are all unidirectional*),

a bidirectional data bus (*note that data line 56 is bidirectional*), a plurality of memory devices, such as eight, (*note the use of up to sixteen exemplary DRAM devices 22*),

a shared command buffer (*note the registers A and B in controller 70, which are connected to each of the plurality of memory devices 22, as explained in column 26, lines 56-57*) coupled between the command and address bus (*18; note that bus 18 comprises, in part, a control bus and an address bus*) and the plurality of memory devices (*22*) for receiving and latching commands and addresses, and

a shared data buffer (*note data buffer 78*) connected between the plurality of memory devices (*22*) and the bidirectional data bus (*18; note that bus 18 comprises, in part, a data bus*) for receiving and latching read data or write data.

As for the claimed pipelined packet protocol, note column 2, lines 34 et seq. and column 20, line 6. [As to the meaning of "pipelined subsystems", it is clear from applicant's specification, page 8, lines 27-30, that this means that each subsystem 130 is pipelined within itself. It does *not* mean that each subsystem is one link in a larger pipeline.]

As for the feature of each memory device containing a column decoder and a row decoder, note column 26, lines 51-57.

As for the feature of each memory device containing a data in buffer and a data out buffer, such was not specifically mentioned in the Katayama et al. system. However the benefits of adding additional levels of buffer hierarchies was well known at the time of the invention. It would have been obvious to include data in and data out buffers for each of the memory devices 22 in the Katayama et al. system. In any case Rosich et al. teaches a DRAM device compatible with the Katayama et al. system and which explicitly teaches a data in buffer and a data out buffer associated with the storage array (note, e.g., Figure 1). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate the DRAM devices of Rosich et al. as the DRAM devices of Katayama et al., since buffers in the Rosich et al. DRAM would have made the timing of the transfer operations to and from the shared buffers more efficient (by latching the data, control or address bits so that such protocols as time sharing could be utilized), especially considering the highly parallel nature of the Figure 9 embodiment of the Katayama et al. system.

At this point it is apparent that the above Katayama et al./Rosich et al. combination teach each and all of the features of *one* of applicant's memory subsystems 130.N. On the other hand, each of applicant's embodiments include a *plurality* of such memory subsystems. In the remarks submitted with the amendment filed January 17, 2002, applicant has now clarified the scope of what is meant by "memory subsystem" (when the specification mentions "each memory subsystem 130" it does *not* mean all of the units which start with "130", it really means "each memory subsystem 130.N", i.e. each *one* of the units surrounded by dashed lines). The combination of references recited above does not specifically mention that memory controller 17 could be connected to *more than one* storage device 16. However, the benefits of adding extra memory were quite well known. Whether extra memory devices 16 were added in parallel, series or in some combinations thereof, it would have been obvious to one having ordinary skill in the art at the time the invention was made to add such extra devices to the Katayama et al./Rosich et al. combination since (1) extra memory meant that more data could be stored, (2) several storage devices 16 linked in parallel would have allowed for faster data retrieval via parallel data transfers, (3) it was noted in St. Regis Paper Co. v Bemis Co. 193 USPQ 8 (7th Cir. 1977) that to duplicate parts for multiple effects is *not* given patentable weight, and (4) the suggestion for plural memory devices is *within the Katayama reference itself* (note column 26, lines 30-45) – in this embodiment the DRAM arrays 22 become part of a larger array of up to 16 devices (in column 9, Katayama explicitly states that "it is preferable that the storage device has a plurality of the DRAM arrays"); consequently, the same motivations exist for integrating the storage device 90 into a larger array of such storage devices.

As to the specific features noted on pages 14-15 of the remarks attached to the amendment of July 1, 2003, the following is further noted:

I. Regarding the load on the command and address bus and the data bus, this is not a question of obviousness. Instead, this is simply a question of physics. In the prior art combination cited above, there are N memory modules connected to a command and address bus, and each of these N memory modules contains one command and address register, one data register and M memory devices. Thus, the total number of memory devices is N X M. The claim language "a first load ... is equal to N devices" is awkward, but is presumed to mean "a first load ... is equivalent to the sum of the loads that would be caused by each of N memory devices" (this interpretation is more accurate, since the loads generated may not necessarily be the same for each memory device).

(A) As for the load on the command and address bus, since each memory module contained only one command and address register, the total number of command and address registers would have been N and since it was the registers (not the memory devices) which were directly connected to the buses, it is the command and address registers that would have determined the load on the command and address bus. Thus, the maximum load would have been equivalent to the sum of the load produced by N memory devices, in a situation where each of the N memory modules has its one command and address register communicating with the command and address bus or data bus at the same time, since the amount of data communicated to the command and address registers was equivalent to the amount of data which would suffice for a single memory device. The registers simply buffered that information and passed it on accordingly.

(B) As for the load on the data bus, since each memory module contained only one data register and since each data register was able to transfer data to or from only one memory device at the same time, the maximum load on the data bus for *each* memory module would have been the load produced by one memory device. Thus, the maximum load on the data bus for *all* memory modules operating at the same time would have been the equivalent of N memory devices. In other words, N x M becomes N x (1 device), which is, of course, N devices.

II. Regarding the use of sockets and connectors to provide the connections already disclosed in the prior art combination cited above, this was well known. In fact, *all manufacturers of data processing machines across the globe used sockets and connectors (pins) to integrate memory components at the time of the invention.* Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to connect the memory components in the Katayama et al./ Rosich et al. combination disclosed above, since this is the only way that these components would have been connected using the elements available on the market at the time of the invention and since such socket/pin connections were well known to be sturdy yet easy to install and remove when necessary.

Response to Amendment

4. With regard to the remarks included on pages 16-19 of the amendment filed on July 1, 2003, these have been carefully considered. However, these are not deemed persuasive for the reasons that follow.

(A) With regard to the first paragraph on page 16, applicant is wrong in concluding that the examiner's assertion on page 5 of the previous Office action regarding the inclusion of additional levels of was a form of official notice, since the cited

motivation to include this feature in the Katayama et al. system relied on the Rosich et al. reference and not simply on the examiner's assertion.

Further, it is not very clear why applicant would request the examiner to "provide a reference that describes such an element" when the Rosich et al. reference was included in the rejection for exactly that purpose. The examiner will be happy to forward another copy of the Rosich et al. reference upon request.

(B) With regard to the second, third, fourth and fifth paragraphs on pages 16 (continuing on pages 17 and 18), the examiner has provided no less than four motivations to combine multiple storage modules of the Katayama et al./ Rosich et al. combination.

(i) Applicant's remarks are non-responsive to motivations (1) and (4).

(ii) As for motivation (2), this was addressed in the fourth paragraph beginning on page 16. The arguments included therein are incorrect for many reasons.

(a) First, applicant argues the benefits of including a plurality of the Katayama et al. memory systems. However, this was not part of the rejection. Instead, the rejection relied on providing a plurality of the cited Katayama et al./ Rosich et al. combination memory systems.

(b) Second, and more importantly, applicant provides no support or technical explanation for why "the load on the buses would be the number of memory devices times the number of memory systems connected to the bus". In fact, in this regard, applicant is completely wrong. The cited Katayama et al./ Rosich et al. combination memory systems each contain the claimed command and address register

(shared command and address buffer) and data register (shared data buffer), both of which reduce the load on the respective buses to the equivalent of one memory device per module, as described above in the rejection.

(iii) As for motivation (3), applicant relies on the argument that "the present invention achieves effects beyond merely duplicating the memory systems". The examiner understands this argument. It is akin to duplicating the tines of a fork. When there is only one tine, the fork can only be used for poking a piece of food. When a second tine is added the fork is not only able to poke up to two pieces of food, but also achieves effects beyond merely poking, such as twirling spaghetti. However, applicant's "achieves effects beyond merely duplicating" argument only carries weight when the effect achieved is unexpected or unobvious. In this case, the effects and benefits of connecting plural memory modules in parallel were not unexpected or unobvious. In fact, the benefits were notoriously well known in the art, for at least the reasons provided in motivations (1), (2) and (4).

Double Patenting

5. The previous obviousness-type double patenting rejections are withdrawn due to the terminal disclaimer filed on July 1, 2003, which correctly details U.S. Patent Nos. 6,286,062 and 6,418,495.

Conclusion

6. This is an RCE of applicant's earlier Application No. 09/434,654. All claims are drawn to the same invention claimed in the earlier application and could have been finally rejected on the grounds and art of record in the next Office action if they had been entered in the earlier application. Accordingly, **THIS ACTION IS MADE FINAL** even though it is a first action in this case. See MPEP § 706.07(b). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no, however, event will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Note: With regard to the request for a telephone interview on page 18 of the remarks attached to the amendment of July 1, 2003, the examiner left a voice message for Tim Clise (#40,957) on July 30, 2003, however no response has been received as of the completion date of this Office action.

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to James Peikari whose telephone number is (703) 305-3824. The examiner is available Mondays to Wednesdays, 10:30 am – 11:00 pm, EST, and on Thursdays from 6:30 am – 10:30 am, EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Kim, can be reached at (703) 305-3821.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (703) 305-3900.

Any response to this action should be mailed to:

Commissioner of Patents and Trademarks

Washington, D.C. 20231

or faxed to:

(703) 746-7239 (Official communications)

or:

(703) 746-7240 (for Informal or Draft communications)

or:

(703) 746-7238 (for After-Final communications)

Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal Drive, Arlington. VA., Sixth Floor (Receptionist).

B. James Peikari
Primary Examiner
Art Unit 2186

August 4, 2003